SYSTEM AND METHOD FOR REDUCING SHORTING IN MEMORY CELLS

Abstract of the Disclosure

An MRAM device includes an array of magnetic memory cells having an upper conductive layer and a lower conductive layer separated by a barrier layer. To reduce the likelihood of electrical shorting across the barrier layers of the memory cells, spacers can be formed around the upper conductive layer and, after the layers of the magnetic memory cells have been etched, the memory cells can be oxidized to transform any conductive particles that are deposited along the sidewalls of the memory cells as byproducts of the etching process into nonconductive particles. Alternatively, the lower conductive layer can be repeatedly subjected to partial oxidation and partial etching steps such that only nonconductive particles can be thrown up along the sidewalls of the memory cells as byproducts of the etching process.

H:\DOCS\BSI\BSI-4654.DOC
101303